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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,005	LI, SHUO-YEN ROBERT	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-35,41 and 42* is/are rejected.

7)☒ Claim(s) *36-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6-15-2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because reference numbers in **FIG. 6B-F, 7,9,10,12-19,44A-C, 69, and 71A-B** because they lack the descriptive legends or labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

   a. Page 114, lines 15, "FIG. 38" should be changed to "FIG. 39",

   b. Page 114, line 18, "FIG. 39" should be changed to "FIG. 40".

Appropriate correction is required.

Claim Objections

3. Claims 17,18,22,24-26,28,31,33,34, and 36-42 are objected to because of the following informalities:

a. Claim 17, line 3, a colon ":" should be inserted following "comprising".

b. Claims 22,36, and 41 are objected for the same reason as stated above in claim 17.

c. Claim 18 recites "..., **n**}" in line 4. For clarity, it is suggested to define what "**n**" is.

d. Claims 22, 36, and 41 are objected for the same reason as stated above in claim 18.

e. Claim 22 recites "**the** guide" in line 4. For clarity, it is suggested to change to "**a** guide".

f. Claim 24 recites "**an** output" in line 2. For clarity, it is suggested to change to "**the** output" since claim 22 has already recited "**an** output" in page 6, line 2. Claim 24 recites "**the** leading bit" in lines 1-2. For clarity, it is suggested to change to "**a** leading bit".

g. Claim 25 recites "**the** leading one bit" in lines 1-2. For clarity, it is suggested to change to "**a** leading one bit".

h. Claim 26 is objected for the same reason as stated above in claim 25.

i. Claim 28 recites, "...the packet is **an idle packet** which is a stream of '0' bits such the packet that the packet is **either a real data packet or an idle packet**..." line 2.

For clarity, it is suggested to revise the claim since an idle packet cannot be either a real data packet or an idle packet.

j. Claim 31 recites "**an** output" in line 2. For clarity, it is suggested to revise "an output" in line 2 since claim 22 also recites "**an** output" in page 6, line 2.

k. Claim 33 recites "**an** output" in line 2. For clarity, it is suggested to revise "an output" in line 2 since claim 22 also recites "**an** output" in page 6, line 2.

l. Claim 34 recites, "**the** second leading one bit" in lines 1-2. For clarity, it is suggested to change to "**a** second leading one bit".

m. Claim 36 recites "**the** guide" in line 4. For clarity, it is suggested to change to "**a** guide". Claim 36 recites, "**the** non-active external input ports" in line 10. For clarity, it is suggested to change to "**a** non-active input ports".

n. Claim 37 recites, "$p_1 \ldots p_r$" in line 3. For clarity, it is suggested to define what "p" is.

o. Claims 38,39,40, and 42 are also objected for the same reason as claim 37 above.

p. Claim 39 recites "the concentrator" in line 4. For clarity, it is suggested to change to "**a** concentrator".

q. Claim 41 recites "**the** guide" in line 4. For clarity, it is suggested to change to "**a** guide".

Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 17, 22 and 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3-5, 9 and 10 of copending Application No. 09/882,112. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 17, 22 and 41 of the instant application merely broadens the scope of the claims 3-5, 9 and 10 of the Patent by eliminating the detailed elements and their functions of the claims. It has been held that the omission an element and its function is an obvious expedient if the remaining elements perform the same function as before. *In re Karlson*, 136 USPQ 184 (CCPA). Also note *Ex parte Rainu*, 168 USPQ 375 (Bd.App.1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Yang (U.S. 5,987,028).

Regarding Claim 17, Yang discloses a method for self-routing a packet (see col. 10, lines 1-30; self-routing the cell) to a given destination address (see FIG. 11 and 20, output address $d_{n-1}\, d_{n-2} \ldots d_0$; see col. 10, lines 9-14) through a network (see FIG. 5, 8, 9, 11 or 20; a bene, batcher, or banyan network), the network being characterized by a guide (see col. 10, lines 5-9; a control sequence: $c_{m-1}\, c_{m-2} \ldots c_0$), the method comprising

generating a routing tag (see FIG. 10, lines 10-14; see col. 17, lines 54 to col. 18, lines 14; routing tag R) for the packet with reference to the guide of the network and the destination address (see col. 10, lines 9-14; a routing tag), and

routing the packet through the network using the routing tag (see col. 10, lines 1-54; see col. 17, lines 54 to col. 18, lines 14).

8. Claims 17-20,22-26,30-32 and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. 6,335,930).

Regarding Claim 17, Lee discloses a method for self-routing a packet (see col. 9, lines 60-65; see col. 10, lines 1-9; self-routing the packet) to a given destination address (see FIG. 2, 6 and 7, destination/output address; see col. 4, lines 9-25; see col. 10, lines 15-25) through a network (see FIG. 6 and 7; NxN network 600 and 700) the network being characterized by a guide (see FIG. 7, the routing bit; see col. 10, lines 5-9), the method comprising

generating a routing tag (see FIG. 8, a routing tag; see col. 9, lines 65-67) for the packet with reference to the guide of the network and the destination address (see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address), and

routing the packet through the network using the routing tag (see col. 10, lines 9 to col. 11, lines 55; routing in accordance with a routing tag).

Regarding Claim 18, Lee discloses wherein the network is a k-stage network (see FIG. 6-7, STG601-STG604, where k=4 stages network) composed of nodes (see FIG. 6-7, switching elements; see col. 8, lines 40-50) and the destination address is expressed as binary ($d_1d_2...d_k$) (see FIG. 6-7, binary output address 111 or 110; see col. 10, lines 15-67) and the guide is expressed as (1), γ (2), . . . , γ(k) (see FIG. 7, the routing bit; see col. 10, lines 5-9) where γ is a mapping from the set [1, 2, . . . , k] (see FIG. 6-7, k=4 stages) to the set [1, 2, . . . , n] (see FIG. 6-7, 601-1 to 601-8, n=8), and wherein the generating a routing tag includes generating binary (see FIG. 8, a routing tag; see col. 9, lines 65-67; see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address).

Regarding Claim 19, Lee discloses prepending binary ($d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(k)}$) to the packet (see FIG. 8, see col. 15, lines 50-60; col. 10, lines 1-49; a routing tag is appended/attached to the packet).

Regarding Claim 20, Lee discloses for a j-th stage node, the routing includes using $d_{\gamma(j)}$ in the j-th stage node to select an output from the j-th stage node to emit the packet, (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than k=4; see FIG. 7, see col. 10, lines 15 to col. 11, lines 55; see col. 17, lines 28-54).

Regarding Claim 22, Lee discloses a method for self-routing a packet (see col. 9, lines 60-65; see col. 10, lines 1-9; self-routing the packet) through a 2^n x 2^n switch (see FIG. 6 and 7; NxN switch 600 or 700), the switch having 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1 b_2 \ldots b_n$, (see FIG. 6 and 7, output ports with binary output address 00,01,10, 11; see col. 8, lines 58 to col. 9, lines 30; see col. 10, lines 9-14) and is composed of a plurality of switching cells (see FIG. 6-7, switching elements; see col. 8, lines 40-50) and interconnected into a k-stage bit-permuting network (see FIG. 6-7, STG601-STG604, where k=4 stages network) which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$ (see FIG. 7, the routing bit; see col. 10, lines 5-9) where γ is a mapping from the set [1, 2, . . . , k] (see FIG. 6-7, k=4 stages) to the set [1, 2, . . . , n] (see FIG. 6-7, 601-1 to 601-8, n=8), wherein each of the switching cells is a sorting cell associated with the partial order "0 (`0-bound`)1 (`1-bound`)" (see FIG. 6-7, 00,01,10 and 11 switching elements in STG600; see col. 8, lines 58-65), the packet being destined for a binary output address $d_1 d_2 \ldots d_n$ (see FIG. 6-7, binary output address 111 or 110; see col. 10, lines 15-67) the method comprising

generating a routing tag $d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(k)}$ (see FIG. 8, a routing tag; see col. 9, lines 65-67; see col. 15, lines 50-60) for the packet with reference to the guide and the destination output address of the packet (see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address), and

routing the packet through the network by using $d_{\gamma(j)}$ in the routing tag in the j-th stage cell, $1 \leq j \leq k$, (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than k=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55; see col. 17, lines 28-54).

Regarding Claim 23, Lee discloses wherein the routing includes removing the bit $d_{\gamma(j)}$ from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$ (see FIG. 2,6, and 7; packet A with routing tag 111, removing the first bit at switching element 704-2 (i.e. 011) before sending the packet; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Regarding Claim 24, Lee discloses wherein the routing includes using the leading bit from the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell to emit the packet(see FIG. 2,6, and 7; packet A with routing tag 111, using the first bit at 704-2 (i.e. 011) before sending the packet to select the output; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Regarding Claim 25, Lee discloses wherein the routing includes removing the leading one bit from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, such that the leading bit of the routing tag is the j-the stage cell, $1 \leq j \leq k$, is always $d_{\gamma(j)}$ (see FIG. 2,6, and 7; packet A with routing tag 111, removing the first bit at 704-2 (i.e. 011) before

sending the packet such that "1" from the roting tag 111 in the stage 704-2 is 011; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Regarding Claim 26, Lee discloses wherein the routing includes rotating the leading one bit of the routing tag of the packet to the end of the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, such that the leading bit of the routing tag in the j-the stage cell, $1 \leq j \leq k$, is always $d_{\gamma(j)}$ (see FIG. 2; see col. 3, lines 60 to col. 4, lines 25; rotating first bit "0" at 001 to 010 at STG201, or rotating first bit "0" at 010 to 100 at STG202; also see FIG. 6-7)

Regarding Claim 30, Lee discloses wherein generating the routing tag includes generating the routing tag $1d_{\gamma(1)}d_{\gamma(2)}\ldots d_{\gamma(k)}$ (see FIG. 8, a routing tag; see col. 9, lines 65-67; and see col. 10, lines 15 to col. 11, lines 60; routing tag which begins with 1, i.e. 111,101, and etc.) for a real data packet (see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address for real/actual data).

Regarding Claim 31, Lee discloses the routing includes using $1d_{\gamma(k)}$ in the routing tag of the real data packet in the j-th stage cell, $1 \leq j \leq k$, (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than k=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55; see col. 17, lines 28-54).

Regarding Claim 32, Lee discloses wherein the routing includes removing the bit $d_{\gamma(j)}$ from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$ (see FIG. 2,6, and 7; packet A with routing tag 111, removing the first bit at 704-2 (i.e. 011) before sending the packet; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Regarding Claim 41, Lee discloses a 2^n x 2^n self-routing switch (see FIG. 6 and 7; self routing NxN switch 600 or 700; see col. 9, lines 60-65; see col. 10, lines 1-9) having an

array of 2^n external input ports (see FIG. 6-7, binary input ports/address; 00,01,10,11) and an array of 2^n external output ports with 2^n distinct binary output addresses in the form of $b_1b_2 \ldots b_n$ for switching a packet (see FIG. 6 and 7, output ports with binary output address 00,01,10, 11; see col. 8, lines 58 to col. 9, lines 30; see col. 10, lines 9-14), the packet being either a real data packet destined for an n-bit binary destination address, or being an idle packet having no pre-determined destination output address (see col. 15, lines 55 to col. 16, lines 40; active/real or idle packet), the switch comprising

a switch fabric (see FIG. 6-7, a combined system of STG601-STG604 or STG701-STG704) with external input ports (see FIG. 6, input ports 601), the switch fabric having a plurality of switching cells (see FIG. 6, 603-1 to 603-4, 604-1 to 604-4,..) interconnected into a k-stage bit-permuting network (see FIG. 6-7, STG601-STG604, where k=4 stages network) which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$ (see FIG. 7, the routing bit; see col. 10, lines 5-9), where γ is a mapping from the set [1, 2, . . . , k] (see FIG. 6-7, k=4 stages) to the set [1, 2, . . . , n] (see FIG. 6-7, 601-1 to 601-8, n=8),

a routing tag circuit, coupled to the external input ports (see FIG. 8, a routing tags are created at the input; see col. 9, lines 65-67), for generating a routing tag $1d_1d_2 \ldots d_n$ (see FIG. 8, a routing tag; see col. 9, lines 65-67; and see col. 10, lines 15 to col. 11, lines 60; routing tag which begins with 1, i.e. 111,101, and etc.) for each of the real data packets with reference to the guide of the bit-permuting network and the destination output address of the packet (see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address for real/actual data), and

a routing control circuit, coupled to the switching cells (see FIG. 15 and 19, input port controller 1502; see col. 16, lines 44-65; see col. 19, lines 60 to col. 20, lines 10), for routing the real data packet through the switch by using $1d_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $1 \leq j \leq k$ (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than k=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Song (U.S. 5,963,554)

Regarding Claim 21, Lee discloses wherein the network is an n-stage network (see FIG. 6, Nx N network), the guide is expressed as $\gamma(1), \gamma(2), \ldots, \gamma(n)$ (see FIG. 7, the routing bit; see col. 10, lines 5-9), where γ is a permutation on the integers from 1 to n and wherein, for a j-th stage node (see FIG. 7, STG702 or STG70, wherein $j \leq n$), the routing includes using in the j-th stage node to select an output from the j-th stage node to emit the packet, $1 \leq j \leq n$ (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than n=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55).

Lee does not explicitly disclose banyan type network. However, Song teaches a banyan type network (see FIG. 3, see col. 5, lines 15-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a banyan type network, as taught by Song in the system of Lee, so that it would provide an effective and improved switching device; see Song col. 1, line 64 to col. 2, lines 49.

Regarding Claim 27, wherein the network is an n-stage network (see FIG. 6, Nx N network), the guide is expressed as $\gamma(1), \gamma(2), \ldots, \gamma(n)$ (see FIG. 7, the routing bit; see col. 10, lines 5-9), where γ is a permutation on the integers from 1 to n and wherein the generating a routing tag includes generating tag $d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(n)}$ (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than n=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55).

Lee does not explicitly disclose banyan type network. However, Song teaches a banyan type network (see FIG. 3, see col. 5, lines 15-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a banyan type network, as taught by Song in the system of Lee, so that it would provide an effective and improved switching device; see Song col. 1, line 64 to col. 2, lines 49.

11. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Kerstein (U.S. 6,058,112).

Regarding Claim 28, Lee discloses wherein the packet is an idle packet which such that the packet is either a real packet or an idle packet (see col. 16, lines 14-30).

Lee does not explicitly disclose a stream of "0" bits. However, Kerstein teaches wherein the packet is an idle packet which is a stream of "0" such that the packet is either a real packet or an idle packet (see col. 6, lines 43-46; control bits "00" indicates that the data is idle). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "00" bits for an idle packet, as taught by Kerstein in the system of Lee, so that it would diagnosed to determine if the switch is working properly, and monitored while it is operating to verify its operation; see Kerstein col. 1, line 34-67 and col. 6, lines 30-67.

Regarding Claim 29, Lee discloses wherein the sorting cell is associated with the partial order "10 (0-bound), 00 (bound), 11 (1-bound)" (see FIG. 6 and 7; STG601 with "10" (for element 603-3), "00" (for element 603-1), and "11" (for element 603-4); see col. 8, lines 58-65. Yang also discloses idle packet

Lee does not explicitly disclose "00 (idle)". However, Kerstein teaches "00 (idle)" (see col. 6, lines 43-46; "00" indicates that the data is idle bound). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "00" for an idle data, as taught by Kerstein in the system of Lee, so that it would diagnosed to determine if the switch is working properly, and monitored while it is operating to verify its operation; see Kerstein col. 1, line 34-67 and col. 6, lines 30-67.

12. Claims 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Yang (U.S. 5,987,028).

Regarding Claim 33, Lee discloses wherein the routing includes using the leading one bit from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-the stage cell to emit the packet (see FIG. 2,6, and 7; packet A with routing tag 111, using the first bit at 704-2 (i.e. 011) before sending the packet to select the output; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Lee does not explicitly disclose leading two bits. However, Yang teaches using the leading two bits of the routing tag (see FIG. 11, (c) 10 101, first two bits "10", c1c0) in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-the stage cell to emit the packet (see col. 10, lines 34-37; see col. 17, lines 54 to col. 18, lines 14). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide leading two bits for routing, as taught by Yang in the system of Yang, so that it would overcome the disadvantages of the prior art by providing the method of assigning routing tag bits for routing signals; see Yang col. 5, line 15 to col. 9, lines 21.

Regarding Claim 34, Lee discloses wherein the routing includes removing the leading one bit from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, such that the leading bits of the routing tag is the j-the stage cell, $1 \leq j \leq k$, is always $1d_{\gamma(j)}$ (see FIG. 2,6, and 7; packet A with routing tag 111, removing the first bit at 704-2 (i.e. 011) before sending the packet such that "1" from the routing tag 111 in the stage 704-2 is 011; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4). Yang discloses leading two bits in routing tag, $1 \leq j \leq k$, such that two leading bits of the routing tag is the j-the stage cell, $1 \leq j \leq k$, is always $1d_{\gamma(j)}$ as described above in claim 33. Thus, the combined system of Lee and Yang discloses removing the second leading one bit from the routing tag for routing.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide leading two bits for routing, as taught by Yang in the system of Yang, for the same motivation as described above in claim 33.

Regarding Claim 35, Lee discloses wherein the routing includes rotating the leading one bit of the routing tag of the packet to the end of the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, such that the leading bits of the routing tag in the j-the stage cell, $1 \leq j \leq k$, is always $1d_{\gamma(j)}$ (see FIG. 2; see col. 3, lines 60 to col. 4, lines 25; rotating first bit "0" at 001 to 010 at STG201, or rotating first bit "0" at 010 to 100 at STG202; also see FIG. 6-7). Yang discloses leading two bits in routing tag, $1 \leq j \leq k$, such that two leading bits of the routing tag is the j-the stage cell, $1 \leq j \leq k$, is always $1d_{\gamma(j)}$ as described above in claim 33. Thus, the combined system of Lee and Yang discloses removing the second leading one bit from the routing tag for routing. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide leading two bits for routing, as taught by Yang in the system of Yang, for the same motivation as described above in claim 33.

13. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Newman (U.S. 5,367,518).

Regarding Claim 42, Lee discloses wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, (see col. 13, lines 35-60; col. 16, lines 60-65; col. 17, lines 50-65; see FIG. 8, routed number; different priorities for different routing numbers are assigned/classified), and wherein the routing tag circuit includes a generator for generating a

routing tag (see FIG. 8, a routing tags are created/generated at the input; see col. 9, lines 65-67), for each of the real data packets of the form $d_{\gamma(1)} \ldots d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag (see FIG. 8, a routing tag; see col. 9, lines 65-67; see col. 15, lines 50-60).

Lee does not explicitly disclose wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$ and $d_{\gamma(1)} p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$. However, Newman teaches wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, (see FIG. 9, Priority Unit 46 with classes 46-0 to 46-(N-1)) wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, (see col. 15, lines 45 to col. 16, lines 15-68; bits in the priority tag) and wherein the routing tag circuit includes a generator (see FIG. 1, Input controller 6) for generating a routing tag for each of the real data packets of the form $d_{\gamma(1)} p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag (see col. 5, lines 57 to col. 6, lines 14; a routing tag and priority tags are created and added to the incoming packets). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide coded priority classes and a tag bit form which consists both routing and priority tags, as taught by Newman in the system of Lee, so that it would provide an improved switching system by utilizing priority tags associated with the routing tag to determine among competing inputs which one or ones will be transmitted through the packet switch; see Newman col. 3, line 40 to col. 4, lines 45.

Allowable Subject Matter

14. Claims 36-40 objected as set forth in paragraph 3, but would be allowable if rewritten to over come the objections.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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